REMARKS

Claims 1-20 are pending in this application of which claims 1, 7 and 17 are independent. Claims 7-20 stand allowed, which is acknowledged with appreciation. Claims 1-6 remain at issue.

The Office Action has rejected claims 1-3 under 35 U.S.C. § 102(b) as being anticipated by Tsujimoto et al. (U.S. Patent No. 4,893,187). Objection has been made to claims 4-6 for being dependent from a rejected base claim, but the claims would be allowable if rewritten in appropriate independent form.

The rejection of claims 1-3 is respectfully traversed.

The present invention, as is recited by claim 1, pertains to an image data conversion device. A portion of claim 1 has been reproduced below for the Examiner's convenience.

> a detection circuit which is connected to said line memory and which *detects the number M of pixels in the horizontal direction* of said first one dimensional data which are stored in said line memory; and
>
> a conversion circuit which is connected to said line memory and said detection circuit and which *reads out, in the order related to said M and, thereby, converts each pixel of said first one dimensional data stored in said line memory into a second one dimensional data* (emphasis added).

Tsujimoto is directed to circuitry for converting first directional run-length codes of an image into second directional run-length codes. The Office Action holds that Tsujimoto at col. 3, line 34 – col. 4, line 18, discloses the invention recited by claim 1. Applicant respectfully disagrees.

Referring to Fig. 1, Tsujimoto illustrates (in block diagram form) the constitution of the apparatus for converting "horizontal runs" into "vertical runs," and operates in the following manner. Run length coding circuit 2 sequentially encodes binary data received from a source (e.g., scanner 1) to provide horizontal run length data to be stored by input

image memory 3. EX-OR processing circuit 6 performs an exclusive OR operation on adjacent lines (j – 1 and j) stored by memory 3 to detect end point coordinate values for a vertical direction, and these values are stored in endpoint coordinate value memory 7. Vertical run conversion circuit 10 converts the horizontal run to a vertical run in accordance with detected endpoints. Detailed explanation of this operation is disclosed at cols. 3 – 6.

Generally, Tsujimoto is directed to the conversion of run length codes in accordance with the EX-OR process circuit 6 detection of an end point of the run length data to be stored by input image memory 3. By contrast, the detection circuit of claim 1 "detects the number of M pixels in the horizontal direction..." Applicant emphasizes that the detection circuit (EX-OR processing circuit 6) of Tsujimoto is incapable of detecting a number of M pixels; rather it can only detect an endpoint coordinate value for the vertical direction. This is at least one fundamental difference between the invention recited by claim 1 and Tsujimoto. Yet claim 1 is even further distinguishable.

The conversion circuit of claim 1 "reads out [data], in the order related to said M and, thereby, converts each pixel of said first one dimensional data...into a second one dimensional data." By contrast, in Tsujimoto the run length coding circuit 13 of the vertical run conversion circuit 10 converts run length codes in accordance with detected end points, and does not convert each pixel. In fact, Tsujuimoto fails to disclose or suggest converting each pixel data from one format to another. This is yet another fundamental difference between the invention recited by claim 1 and Tsujimoto.

These fundamental differences are further illustrated by Tsujimoto, who claims to avoid converting "every pixel" from one format to another for determining vertical run length codes. (See col. 1, lines 41-58). Taking into consideration the full disclosure of

Tsujimoto, it is clear that Tsujimoto fails to identically teach each and every element of claim 1.

Regarding claim 2, it follows that Tsujimoto fails to disclose or suggest a detection circuit that "includes a circuit which reads out data representing the pixel number M in the horizontal direction from said first one dimensional data," as this claim recites. Rather, as discussed above, EX-OR processing circuit 6 of Tsujimoto merely detects an end point. The invention recited by claim 2 is fundamentally different from the detection circuitry of Tsujimoto.

Regarding claim 3, Tsujimoto fails to disclose or suggest "a conversion circuit [that] includes a circuit which reads out each pixel of said first one dimensional format in the order in accordance with a multiple of M," as this claim recites. The text cited by the Office Action (col. 4, lines 9-16) has little or no relevance. There is no disclosure of reading out "each pixel." Rather, the text focuses on reading end points. Also, it follows that since there is no disclosure of determining M, the conversion circuit (vertical run conversion circuit 10) is incapable of reading out each pixel in accordance with a multiple of M. The invention recited by claim 3 is fundamentally different from the conversion circuitry of Tsujimoto.

Because the Tsujimoto fails to identically disclose each and every element of claims 1-3, the rejection is improper and withdrawal thereof is respectfully solicited. Likewise, withdrawal of the objection to claims 4-6 is respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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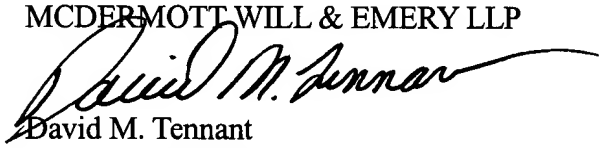

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